IN THE ABSTRACT

Please delete the abstract and replace it with the following:

An architecture and distributed hierarchical interconnect scheme for field programmable gate arrays (FPGAs). The FPGA is comprised of a number of cells that perform logical functions on input signals. A set of block connectors are used to provide connectability between cells and accessibility to a hierarchical routing network. Uniformly distributed layers of routing network lines are used to provide connections. Switching networks provide connectability between the routing network lines. Additional uniformly distributed layers of routing network lines are implemented to provide connectability between different prior layers of routing network lines. Programmable bi-directional passgates are used as switches to control which of the routing network lines are to be connected.